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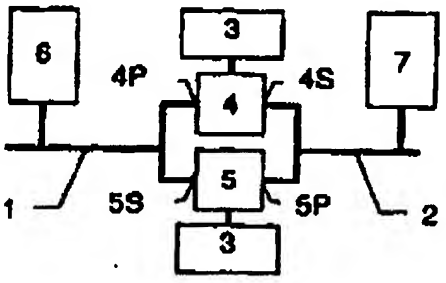
(54) Title: DATA TRANSFER ASSEMBLY

(57) Abstract

Data transfer assembly comprising a primary (1) and a secondary (2) bus for electronic, digital data signals adapted to a predetermined standard, e.g. a PCI local bus, at least two electronic memory devices (3) of any known type, and means for storing and down-loading of the electronic data to and from said busses (1, 2), which also comprises at least two control devices (4, 5), e.g. a i960®RP processor from Intel®, adapted to said standard, each said control device having three ports of which: the first port is connected to one of the said memory devices (3) for loading and unloading of data to and from said memory device; the second and third ports (4P, 4S, 5P, 5S) are connected to said primary and secondary busses (1, 2) and are capable of communication with said primary and secondary busses using said standard; each control device (4, 5) being capable of loading data received from the busses, and transmitting downloaded data to the said busses (4, 5); the said control devices comprise a communication bridge, e.g. a PCI to PCI bridge, between its ports (4P, 4S, 5P, 5S), providing data communication between the primary and secondary busses.



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DATA TRANSFER ASSEMBLY

This invention relates to a data transfer assembly comprising two busses, (from now referred to as the primary and secondary bus) for electronic, digital data signals adapted to a predetermined standard, e.g. a PCI local bus, at least two electronic memory devices of any known type connected to said primary bus for storing and down-loading of the electronic data, and to said secondary bus for transmitting the downloaded data.

The present invention relates to systems using the VMEbus, which is a standard used for interconnecting different types of apparatus, e.g. for data acquisition and processing. The different electronic devices are built as modules adapted to specific physical and electrical requirements, and communicating with each other using the VME bus. Thus the different modules may be bought from different vendors, and still work together. Each module in this system may in its turn comprise modules according to another standard, the PMC (PCI Mezzanine Cards). PCI (Peripheral Component Interconnect) local bus is a data bus provided by Intel® also comprising protocols for communication between different components in a system. The PCI local bus has a peak bandwidth of 132 Mbytes/second. It is also meant to provide "Plug & Play" operation for add-in boards.

A main object to this invention is to provide a system for handling data in applications with high bandwidth requirements, using a PCI local bus. Examples of such applications may be transmitting signals received from a camera to be stored on one or more disks, or digitized data from a A/D (analog to digital) converter to a filtering device.

A suggested solution in a data acquisition system has been the use of two memories being loaded and emptied of data in an alternating fashion, by loading one of the memories while at the same time unloading the other and switching at convenient intervals, and thus making a so called "swinging buffer". This has the advantage of allowing varying data transfer rates, as well as giving room for data processing on continuous streams of data.

Known systems using this technique comprises a first I/O module receiving data and transmitting these data to a first memory. When the first memory module has been filled the data passing the I/O module is transmitted to the second memory module, and at the same time the data in the first memory is transmitted to a second I/O module which may forward the data e.g. to a processor. In previous systems using this technique the modules where connected using VME bus and/or VSB (VME Sub-system Bus), and were therefore limited to less than 40 MB/s. Using the same concept in a system based upon the PCI local bus a transfer speed of more than 100 MB/s is achieved.

In practice it was found that the system described above would have to use PMC modules to handle the data from the primary and secondary bus, a controller to control the loading and unloading of each memory and a PCI-PCI bridge to secure correct communication between the PCI local bus on the two sides of the system. This is a complicated system which is difficult to make sufficiently compact to be implemented in a local PCI subsystem on a VMEbus module.

It is an object of this invention to provide a compact I/O-system being capable of transferring data at a speed of more than 100 MB/s. It is also an object of this invention to provide a compact I/O-system being adapted to be used in an existing PCI or related system, the PCI system optionally being a subsystem in a VMEbus system.

The objects of this invention are achieved using an assembly characterized that it also comprises at least two control devices, e.g. a i960®RP processor from Intel®, adapted to said standard, each said control device having three ports of which the first port is connected to a block of memory devices for alternately loading and unloading of data to and from said memory block, the second and third ports are connected to said primary bus and secondary bus and are capable of communication with said primary bus and secondary bus using said standard, each control device being capable of loading data received from the primary bus, and transmitting downloaded data to the secondary bus, the said

second and third port in each of the said control devices comprising communication bridge, e.g. a PCI to PCI bridge, providing data communication between the primary and secondary bus, and having a primary and a secondary port.

According to a preferred embodiment of the invention the predetermined standard is PCI local bus or equivalents and the assembly comprises a first and a second control device, each having a third port connected to a memory device, said primary port of the first control device being connected to said primary bus and said secondary port being connected to the secondary bus, said primary port of the second control device being connected to said secondary bus and said secondary port being connected to the primary bus. This embodiment provides a symmetric circuit for equally good communication both ways through the assembly.

The invention will now be described by way of example referring to the accompanying drawings:

Figure 1 is a diagram showing the structure according to the present invention.

Figure 2 is a diagram showing an application example; a data recorder with multiple SCSI disks.

Figure 3 is a diagram showing a second application example; a data acquisition system with DSP.

Figure 1 gives a schematic view of the invention, having two blocks of memory devices 3 each coupled to a third port on a control device 4,5. The block of memory devices may be built from any available random access memory device such as DRAM and SRAM. Typical memory sizes for each of the two memory blocks starts at 4MB, with an upper limit defined by the available technology, currently 1GB.

The control devices 4,5 comprise three ports, one being connected to the memory block 3 and the other two 4P,4S,5P,5S being connected to the primary 1 and secondary 2 busses, respectively. The control devices are adapted to loading and unloading the memory block with data to and from devices 6,7 connected to the primary and secondary busses,

to and from the memory block connected to the third port of each control device. The control devices 4,5 also each comprises a bridge between the second and third ports providing communication between the two ports 4P,4S,5P,5S as well as a possibility to process the data, and to synchronize and control the data flow. The communication bridges each comprise a primary 4P,5P and a secondary 4S,5S port.

In addition to the bus bridge, the control devices 4,5 may preferrably also comprise a micro-processor core, memory controller, means of address translation, messaging unit, DMA controllers and other peripheral interfaces. The control devices 4,5 may also comprise means for communication with each other using the PCI local bus, in order to co-ordinate the loading and unloading of data from the memory devices 3 and optimize the data transfer through the assembly. In this way the control devices may choose to switch from loading to unloading and vice versa before the memory devices are full or empty, depending on the data and control signals transmitted from other circuits 6,7 in the system in which the invention is used.

The other circuits 6,7 connected to the busses may be using a data bus of any suitable kind. The data bus will, however, preferably be a PCI local bus or a related standard for communication between different electronic circuits. The interfaces are adapted for transmitting signals to and from the circuit according to the invention.

Figure 2 and 3 present diagrams of configurations in which the invention may be used.

Figure 2 shows a system where digital data is received from a camera 8 and is transferred to one of the memo. blocks 3 by one PMC module 6, using the primary PCI b 1. Multiple SCSI controller PMC modules 7a,7b,7c connecte_ to the secondary PCI bus moves the data from the memory to multiple SCSI disks 9a,9b,9c. (SCSI is a widely used standard for storage devices such as hard disks.) An assembly according to the invention 3,4,5 (see figure 1) is used to control the flow of data to the disks 9a-9c.

The example in figure 3 shows a data acquisition system where analog data from e.g. a sonar is digitized in an external A/D converter 12, and fed into one memory block 3 through a parallel input PMC module 6 connected to the primary bus 1, using the PCI bus protocol. On the secondary bus 2 a PMC module 7 with a DSP (digital signal processor) performs an initial filtering of the data which is transmitted to a main DSP engine 11. The A/D converter 12, the card comprising the assembly according to the invention and the main DSP engine 11 may all be connected to a VME bus, which typically is used for communication between the data acquisition system and a host processor also connected to the VMEbus.

Other devices used in connection to the assembly may be of any kind as long they conform to the related standard. Such devices include:

- Bus-to-Bus Bridge (chips and modules) for connection to standard busses such as RACEway, SCI, PCI, VMEbus, VSB.
- A/D Converter (chips and modules).
- Parallel I/O device (chips and modules).
- Storage controller (chips and modules) for e.g. SCSI.
- Network interface (chips and modules) for connection to standard networks such as Ethernet, ATM, FDDI, Fiber Channel.
- DSP processor (chips and modules).
- Frame grabber (chips and modules).
- Graphics (chips and modules).

C l a i m s

1. Data transfer assembly comprising a primary (1) and a secondary (2) bus for electronic, digital data signals adapted to a predetermined standard, e.g. a PCI local bus, at least two electronic memory devices (3) of any known type, and means for storing and down-loading of the electronic data to and from said busses (1,2),
c h a r a c t e r i z e d in that it also comprises at least two control devices (4,5), e.g. a i960®RP processor from Intel®, adapted to said standard, each said control device having three ports of which:
the first port is connected to one of the said memory devices (3) for loading and unloading of data to and from said memory device,
the second and third ports (4P,4S,5P,5S) are connected to said primary and secondary busses (1,2) and are capable of communication with said primary and secondary busses using said standard,
each control device (4,5) being capable of loading data received from the busses, and transmitting downloaded data to the said busses (4,5),
the said control devices comprises a communication bridge, e.g. a PCI to PCI bridge, between its ports (4P,4S,5P,5S), providing data communication between the primary and secondary busses.

2. Assembly according to claim 1,
c h a r a c t e r i z e d in that the predetermined standard is PCI local bus or equivalents and the assembly comprises a first and a second control device (4,5), each having a third port connected to a memory device (3),
said primary port (4P) of the first control device (4) being connected to said primary bus (1) and said secondary port (4S) being connected to the secondary bus (2),
said primary port (5P) of the second control device (5) being connected to said secondary bus (2) and said secondary port (5S) being connected to the primary bus (1).

3. Assembly according to claim 1 or 2, c h a r a c t e r i z e d in that the control devices (4,5) are capable of communication with each other to co-ordinate the loading and unloading of data in the memory devices (3).

4. Assembly according to one of the preceding claims, c h a r a c t e r i z e d in that the assembly is adapted to receiving data using the primary bus (1) and transmitting data using the secondary bus (2),

and alternatively loading the first memory device with data received from the primary bus (1) and transmitting data from the second memory device through the secondary bus (2) and vice versa.

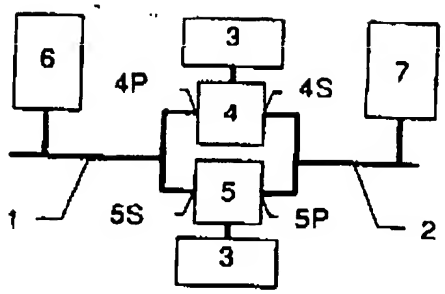


Figure 1

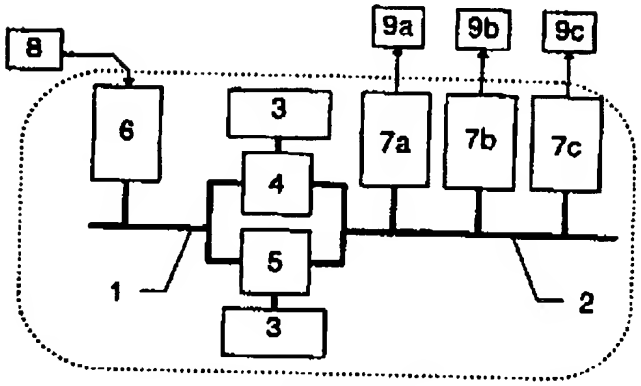


Figure 2

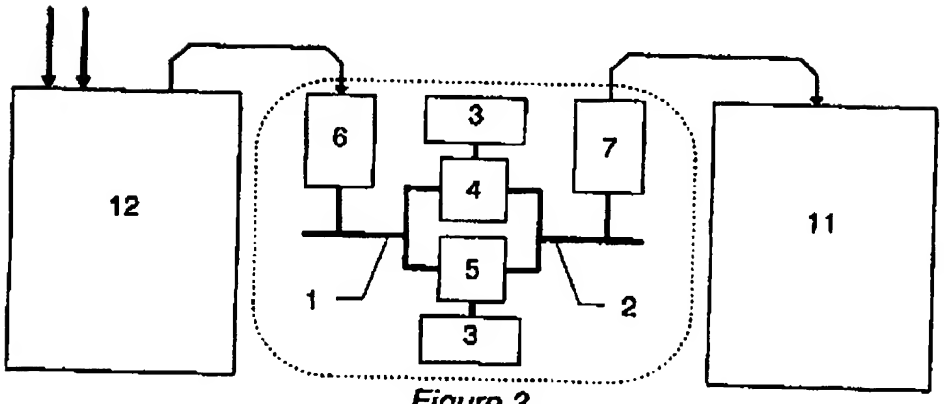


Figure 3

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# INTERNATIONAL SEARCH REPORT

International application No.
PCT/NO 97/00007

## A. CLASSIFICATION OF SUBJECT MATTER

IPC6: G06F 13/38
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## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: G06F

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SE,DK,FI,NO classes as above

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## C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| A | EP 0629956 A2 (INTERNATIONAL BUSINESS MACHINES CORPORATION), 21 December 1994 (21.12.94) | 1 |
| A | US 5502822 A (MAKOTO TAKEBE), 26 March 1996 (26.03.96) | 1 |
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